CLAIMS:

1. An integrated circuit (1), having a substrate (3) and having a signal-processing circuit (4), which signal-processing circuit (4) is produced in a region of the substrate (3) adjoining a surface (8) of the substrate (3) and has a plurality of circuit elements (5, 6, 7) and at least one first contact pad (9), wherein the first contact pad (9) has a first boundary face (10) accessible from outside the substrate (3) and a second boundary face (11) opposite from the first boundary face (10), wherein the first contact pad (9) is intended for the electroconductive connection of a component contact (2) of a circuit component external to the integrated circuit (1) to the signal-processing circuit (4), and having a protective layer (12) that is electrically insulating and provided on the surface (8) of the substrate (3) to protect the regions of the integrated circuit (1) covered by said protective layer (12), wherein for each first contact pad (9) an aperture (13) in the protective layer (12) is provided, wherein for each first contact pad (9) a second contact pad (14) is provided that is of a height (h) of at least 15 μm and is intended for direct connection to a component contact (2) and extends through the relevant aperture (13) to the first contact pad (9) and is electroconductively connected to the first contact pad (9) and is seated on the protective layer (12) by an overlap zone (z) that projects laterally beyond the aperture (13) and is closed on itself like a ring, wherein, along the whole of its ring-like extent, the overlap zone (z) projects beyond the aperture (13) laterally by substantially the same width of overlap (w), wherein the width of overlap (w) is in a range of between 2 μm and 15 μm, and wherein at least one element (5) of the signal-processing circuit (4) is provided opposite the second boundary face (11) of the first contact pad (9).

2. An integrated circuit (1) as claimed in claim 1, wherein only one capacitor (5) belonging to the signal-processing circuit (4) is provided opposite the second boundary face (11) of the first contact pad (9).

3. An integrated circuit (1) as claimed in claim 2, wherein the planar shape of the capacitor (5), which planar shape extends parallel to the surface (8) of the substrate (3), and the planar shapes of the second contact pad (14) and the aperture (13), which planar shapes

also extend parallel to the surface (8) of the substrate (3), are substantially the same, and the area of the planar shape of the capacitor (5) is at most 10% larger than the area of the planar shape of the second contact pad (14).

4. An integrated circuit (1) as claimed in claim 2, wherein the capacitor (5) is formed by a multilayer capacitor.

5. An integrated circuit (1) as claimed in claim 2, wherein at least one metal layer (26, 27) is provided between the first contact pad (9) and the capacitor (5) as a mechanical protective layer for the capacitor (5).

6. An integrated circuit (1) as claimed in claim 2, wherein the first contact pad (9) comprises at least two metal layers (28, 29) that are connected together electrically and mechanically by electroconductive bridges (31).

7. An integrated circuit (1) as claimed in claim 1, wherein the width of overlap (w) is of a nominal value of 7 μm.